DEEP-TECH PATENTS • SECTION 3(K) PRACTICE

Patenting Enterprise AI and Cloud Architectures in India

Demystifying Section 3(k) 'Computer Program Per Se' Exclusions, 'Further Technical Effect' Rules, and High Court IPD Jurisprudence

Author: Gaurav Arora, Advocate & Regd. Patent Agent | Chambers of Gaurav Arora (New Delhi / Gurugram) | www.aroraipcounsel.com

Executive Summary & Takeaway: Executive Strategy: A widespread misconception among Indian software founders and engineering leaders is that software and artificial intelligence inventions cannot be patented in India. While Section 3(k) of the Patents Act, 1970 excludes 'a computer programme per se,' Parliament's deliberate inclusion of the qualifying phrase 'per se' ensures that software is patentable when it achieves a 'technical effect' or 'technical contribution.' Following landmark Delhi High Court IP Division rulings (Ferid Allani, Microsoft, and Ericsson v. Lava), software that optimizes hardware resources, accelerates distributed data processing, or improves cryptographic security clears statutory eligibility.

1. Deconstructing Section 3(k) 'Per Se'

The Joint Parliamentary Committee (2001) added 'per se' to Section 3(k) to avoid barring genuine technological inventions implemented in software. In *Ferid Allani v. Union of India (DHC 2019)* and *Microsoft Technology Licensing (DHC 2023)*, the Delhi High Court affirmed that software is eligible for patent protection if it demonstrates a technical effect, such as improved hardware efficiency, novel memory allocation, or technical data transformation.

2. The 7 Stambhas of Indian Patent Examination

In *Lava International v. Ericsson (DHC 2024)*, the High Court established the 'Seven Stambhas' (pillars) of patentability. Level 2 eligibility exclusions (Section 3) must be analyzed independently of Level 3 prior art obviousness. An AI pipeline that controls physical processing nodes or transforms raw sensor data clears Section 3(k) on its technical contribution alone.

3. Hypothetical Case Study: TensorEdge Systems (Bengaluru / Gurugram)

TensorEdge developed a distributed edge-computing framework optimizing LLM inference latency across heterogeneous GPUs. The patent examiner rejected the claims under Section 3(k) as an abstract mathematical algorithm. By restructuring the claims into a hardware-software nexus—specifying memory cache eviction algorithms, kernel thread scheduling, and quantitative 42% latency reduction—counsel overcame the FER objection and secured a grant without an oral hearing. This demonstrates that framing technical effect is decisive in CRI prosecution.

4. 4-Step Claim Drafting Protocol for AI & Cloud Startups

1. **Avoid Pure Algorithmic Claims:** Never claim raw mathematical models or business logic in isolation.
2. **Anchor in Concrete Technical Interaction:** Express methods in terms of processor state changes, cache synchronization, or memory latency.
3. **Harmonize with US § 101 Step 2B:** Draft specifications satisfying both US Alice Step 2B (inventive concept) and Indian Section 3(k) (technical contribution).
4. **Highlight Empirical Technical Benchmarks:** Include comparative performance graphs proving processing efficiency and resource optimization.

About the Author & Chambers

Gaurav Arora is an Advocate (Bar Council of Delhi) and Registered Indian Patent Agent (INPA-1900), serving as Founder and Lead Arguing Counsel at Arora IP Counsel (Chambers of Gaurav Arora) in New Delhi / NCR. He holds an LL.M. in Intellectual Property Law from Benjamin N. Cardozo School of Law, New York (Dean’s Merit Scholar), a B.E. in Mechanical Engineering from Punjab Engineering College (PEC Chandigarh), an LL.B. from GLC Mumbai, and passed the USPTO Patent Bar Examination (2016). He is the author of the statutory treatise "Patently Obvious COMMA: Correct Interpretation of the Patents Act, 1970" (2023), deposited in the permanent collection of the WIPO Knowledge Center in Geneva.

Practice Portal & Directory: www.aroraipcounsel.com | Correspondence: gaurav@aroraipcounsel.com

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